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Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to clarify Applicants invention.

Support for the amended claims are found in the original claims and/or the Specification. No new matter has been added.

For example support for the amended claims and new claim 20 is found in the Figure 3, and in the Specification at paragraph 0028 and 0029:

"As previously described, process for erasing a flash memory cell is reverse of the programming process. That is, erasing of a flash memory cell is performed by removing or transferring a sufficient charge (below a predefined threshold level) from the floating gate 122. In one embodiment, a polysilicon to polysilicon tunneling technique is used for erasing. In this technique, a positive voltage ranging from about +10 volts to about +15 volts is applied to the control gate 129, and a reference potential of

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approximately 0 volts is applied to the P+ source 114 and to the P+ drain 116, thereby causing removal of electrons from the floating gate 122."

"FIG. 2 is an illustrative cross-sectional diagram of a split-gate, P-channel flash memory cell 200 having a tip, according to an embodiment. The structure and operation of the memory cell 200 is substantially similar to the memory cell 100 except as noted below. For example, the shape and thickness of elements such as the floating gate 122, and the control gate 129 are different. An additional polysilicon layer 210 having a double concave surface is positioned between the floating gate 122 and the first layer 120. In the depicted embodiment, the thickness of the floating gate 122 and the thickness of the polysilicon layer 210 below the floating gate 122 is variable. In the depicted embodiment, the floating gate 122 has a matching double convex surface resulting in the formation of a tip 222. The tip 222 advantageously produces a stronger electric field compared to the memory cell 100 resulting in a faster and more efficient erasing of the cell 200."

And at paragraph 0029:

FIG. 2 is an illustrative cross-sectional diagram of a split-gate, P-channel flash memory cell 200 having a tip, according to an embodiment. The structure and operation of the memory cell 200 is substantially similar to the memory cell 100 except as noted below. For example, the shape and thickness of elements such as the floating gate 122, and the control gate 129 are different. An additional polysilicon layer 210 having a double concave

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surface is positioned between the floating gate 122 and the first layer 120. In the depicted embodiment, the thickness of the floating gate 122 and the thickness of the polysilicon layer 210 below the floating gate 122 is variable. In the depicted embodiment, the floating gate 122 has a matching double convex surface resulting in the formation of a tip 222. The tip 222 advantageously produces a stronger electric field compared to the memory cell 100 resulting in a faster and more efficient erasing of the cell 200.

Claim Rejections under 35 USC 103

1. Claims 1-4 and 11-14 stand rejected under 35 USC 103(a) as being unpatentable over Chang et al. (US 5,706,227) in view of Lojek (US 6,822,285).

Chang et al. disclose a P-channel MOS memory cell with a select and control gate (see Figure 1, item 25 and 26) overlying a floating gate (see item 22) where the select and control gate is separated from the floating gate by an insulator layer (item 28) and the floating gate (22) is separated from the channel region by a tunnel oxide (item 24) (see Abstract). The operation of the memory cell of Chang et al. is by hot electron injection from the drain end of the channel region to the floating gate.

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Erasing is accomplished by electron tunneling from the floating gate to the channel region (N-well) (see Abstract; col 2, lines 39-54).

Thus, the principle of operation is impact ionization of holes accelerated toward the drain region to create hot electrons, which are then attracted (tunnel through) to the floating gate.

Thus, Chang et al. disclose a device having a different structure and that is differently operable than the device and method of Applicants.

Chang et al. nowhere disclose polysilicon to polysilicon tunneling or disclose that an erase operation could be accomplished by polysilicon-polysilicon tunneling or disclose a floating gate comprising an interface for the polysilicon-polysilicon tunneling.

Lojek on the other hand, discloses a multi-element floating gate structure that may be charged by band-to band tunneling **without a control gate** (see Abstract). The multi-element floating gate structure of Lojek has a central polysilicon gate

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portion with **polysilicon spacers** formed adjacent the central portion and **separated by a tunnel oxide layer** (see Abstract; Figure 8, items 67 and 69; col 5, lines 8-22). A third polysilicon layer (item 77; Figure 13) is formed over the both the central portion and the spacers **to provide a common electrical connection** (col 5, lines 53-60). Lojek teaches that the formation of the polysilicon spacers increases the probability of electron capture **by electrons tunneling from the substrate (silicon) across the tunnel oxide to either the central polysilicon portion or the polysilicon spacers** (col 1, lines 52-67; col 2, lines 53-61; col 5, lines 8-22).

Thus Lojek disclose a significantly different structure than either Chang et al. or Applicants disclose and claimed invention and there is no reason to expect that the structure of Lojek who **does not disclose a control gate or a control and select gate** would be similarly operable as the structure of Chang et al.

Nowhere does Lojek disclose a control or a select gate or **that an erase operation may be accomplished by polysilicon-polysilicon tunneling** or disclose that the multi-element floating gate structure can accomplish an erase operation by applying a positive voltage bias to a control gate structure, or disclose a

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floating gate including a second top polysilicon portion.

Even assuming *arguendo* a proper motivation for combining Change et al. and Lojek, which apparently is found only in Applicants disclosure, such combination does not produce Applicants disclosed and claimed invention.

Examiners assertion that a polysilicon-polysilicon tunneling technique is well known in the art is respectfully rejected by Applicants, and note that Examiner has provided no support for this assertion.

Nowhere do the combined references disclose or suggest"

"a polysilicon floating gate comprising a lower portion and a top portion to form a polysilicon-polysilicon interface, said floating gate disposed over the first insulating layer, wherein the floating gate is positioned over a first portion of the channel region but not a second portion of the channel region;"

or

"wherein the cell is operable to be programmed by a band-to-band hot electron (BBHE) technique and erased by a polysilicon to polysilicon tunneling technique comprising said interface."

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"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

2. Claims 5-10 and 15-19 stand rejected under 35 USC 103(a) as being unpatentable over Chang et al. (US 5,706,227) in view of Tran et al. (USPUB 2004/0125653).

Applicants reiterate the comments mad above with respect to Chang et al. and Lojek (Examiner has not explicitly applied Lojek, and Applicants assume this is an error since claim 5 is dependent on claim 1 and claim 15 is dependent on claim 11).

The fact that Tran et al. disclose that the floating gate has a poly tip structure that points to the control gate to enhance the electric field in an erase operation using **Fowler-Nordheim (FN) tunneling** with respect to a **source side injection** (SSI) flash memory cell, where a bias applied only to source side, does not further help Examiner in establishing a *prima facie* case of obviousness (see paragraph 0019 and 0020; paragraph

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0123; 0124).

Even assuming *arguendo* a proper motivation for combination of the cited references, such combination does not produce Applicants disclosed and claimed structure and operation.

The combined references do not teach Applicants method and structure where such structure is operable as Applicants have disclosed and claimed:

"a polysilicon floating gate comprising a lower portion and a top portion to form a polysilicon-polysilicon interface, said floating gate disposed over the first insulating layer, wherein the floating gate is positioned over a first portion of the channel region but not a second portion of the channel region;"

or

"wherein the cell is operable to be programmed by a band-to-band hot electron (BBHE) technique and erased by a polysilicon to polysilicon tunneling technique comprising said interface."

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The

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teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

With respect to claims 8 and 9 and 18 and 19, Examiners assertion a P+ drain coupled to a bit line and a control gate is coupled to a word line is "well known" is respectfully rejected by Applicants, and note that Examiner has provided no support for this assertion. Rather the **control and select gate** of Chang et al. shows that this is not the case i.e., where the control gate is used to select or unselect the cell.

Conclusion

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

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In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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